B3 cont.

10. The device of claim 9 further comprising a grounded wiring layer provided on the backside of the substrate,

wherein the conductor film is connected to the grounded wiring layer. --

**REMARKS**

The Examiner's final Office Action of November 4, 2002 has been received and its contents reviewed. Applicants would like to thank the Examiner for the consideration given to the above-identified application.

Claims 1-7 were pending prior to this amendment. By this Amendment claims 1 and 6 have been amended, and new claims 8-10 have been added. Accordingly, claims 1-10 are pending for consideration in the present application, of which claims 1, 6, and 9 are independent. In view of the actions above and the remarks below, reconsideration and allowance of the pending claims are respectfully requested.

Referring now to the detailed Office Action, claims 1, 3, 4, and 6 stand rejected under 35 U.S.C. §102(b) as anticipated by Fujita et al. (U.S. Patent No. 5,485,039 – hereafter Fujita). Further, claims 2, 5, and 7 stand rejected under 35 U.S.C. §103(a) as unpatentable over Fujita.

As amended, claim 1 further recites a conductor film formed on the inside faces of the through holes. According to claim 1, the multiple through holes between the two semiconductor components enable a reduction of electric interference, particularly interference by radio frequency (RF), more effectively than in a case of one through hole between the components.

On the other hand, Fujita et al. discloses only a semiconductor device having an active device, such as transistors 2, and wiring conductor 3 on a semiconductor substrate 1 cooperating with the active devices 2, conductive pins 6 inserted through holes 5 to deliver electrical signals to and from electrical circuits, as shown in Fig. 1. Further, the conductive pins 6 are connected to the wiring conductor 3 by leads 7, and the through holes 5 are filled with adhesive 8 to fix the conductive pins 6 in the through holes, as disclosed in col. 4, lines 17-42 of Fujita.

In Fig. 10 of Fujita, another embodiment shows an insulation film 16 and a low-melting point metal filler 17 in through holes 5 to fix the position of the conductive pints 6. Further, as

disclosed in col. 6, lines 26-27, the low-melting point metal filler ensures the electrical connection of the wiring conductors 3 and conductive pins 6. The low-melting point metal filler 17 of Fujita is filled into through holes having insulation film 16 so that insulation of the metal filler can be obtained. Applicants respectfully assert that, to ensure insulation, the insulation film 16 desirably has a certain thickness. However, the existence of the insulation film with a thickness causes the region where the metal filler 17 occupies to become smaller, hence, increasing the leakage of RF. Therefore, the low-melting point metal filler 17 in Fig. 10 of Fujita cannot provide RF shielding.

Applicants respectfully assert that Fujita does not disclose a conductor film formed on the side faces of the through holes as recited in amended claim 1, as well as amended claim 6. Moreover, the leads 7 of Fig. 1 and the low-melting point metal filler 17 of Fig. 10 are for conducting electrical signals between electrical components and **not** for reducing radio frequency interference. As the through holes 5 of Fujita are for housing the conductive pins 6 and/or low-melting point metal filler 17, Fujita does not teach or suggest their use for reducing RF interference.

Should the Examiner still asserts that through holes 5 of Fujita are for reducing RF interference or that Fujita discloses a conductor film formed on the side faces of the through holes, Applicants would respectfully request the Examiner to provide specific support for such assertion.

Furthermore, in the structure of Fig. 1 of Fujita, in order to keep insulation between the substrate and the leads 7, it is desirable that the through holes are contact with the leads 7 as little as possible. That is to say the leads 7 should to be thin. However, the leads for the through holes lessens the shield effect of radio frequency, and as a result, interference by radio frequency cannot be prevented. Hence, at least in the embodiment of Fig. 1, Fujita teaches away achieving the effect of the claimed invention.

With respect to amended independent claim 6, it is clarified that the first group of through holes is different from the second group of through holes, and, moreover, that the conductor film is provided on a side surface of each through hole ad thereby noise in isolation between adjacent

components can be reduced by at least either the first group of through holes or the second group of through holes.

Consequently, since each and every feature of the present claims is not taught (and is not inherent) in the teachings of Fujita, as is required by MPEP Chapter 2131 in order to establish anticipation, the rejection of claims 1, 3, 4, and 6 under 35 U.S.C. §102(b), as anticipated by Fujita. is improper and should be withdrawn.

With respect to the §103(a) rejection, Applicants respectfully submit that the amendments and arguments set forth above in relation with the §102(b) rejection are also applicable. Accordingly, Applicants also request reconsideration and withdrawal of the §103(a) rejection.

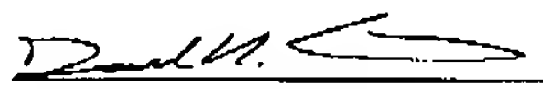
According to the invention recited in new claim 8, it is possible to enlarge a region where interference by the radio frequency is reduced in a vertical surface to a stream of current, namely a cross-sectional area of the through holes, and to keep a strength of the substrate.

According to the invention recited in new claim 9, by providing the conductor film on the side surface of the through holes, noise in isolation between the adjacent components can be reduced without deepening a depth of the through holes, more specifically without decreasing a g/d ratio in Fig. 2. The reason is that the conductor film provided on the side surface of the through holes fulfills a role of a shield for the RF, substantially isolation between the components.

Support for the amendment of claim 1 can be found at least in, e.g., Fig. 1 of the present application; support for the amendment of claim 6 can be found at least in, e.g., Fig. 5 and Embodiment 3, in pages 10-13, of the present specification; support for new claim 8 can be found at least in Fig. 1 of the present application; and support for new claims 9 and 10 can be found at least in, e.g., Fig. 3 and Embodiment 2, in pages 8-10, of the specification.

Having responded to all rejections and objection set forth in the outstanding non-Final Office Action, it is submitted that claims 1-10 are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,



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**MARKED UP VERSION OF AMENDMENTS**

1. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate;

[at least] two semiconductor components provided on the principal surface of the surface; and

multiple through holes, which pass from the principal surface through the backside of the substrate and are provided in a region of the substrate between the [at least] two components so as to substantially eliminate the electrical interference between the two semiconductor components; and

a conductor film formed on the side faces of the through holes.

6. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate;

at least two semiconductor components provided on the principal surface of the substrate;

electrodes of the at least two components provided on the substrate so as to substantially eliminate the electrical interference between the two semiconductor components;

a first group of through holes, which pass from the principal surface through the backside of the substrate and are provided in respective regions of the substrate under the electrodes;

a first conductor film provided on the side faces of the first group of through holes;

a second group of through holes, which differ from the first group of through holes, which pass from the principal surface through the backside of the substrate between the components;

a second conductor film provided on the side faces of the second group of through holes; and

a wiring layer, which is provided on the backside of the substrate and is in contact with the first and second conductor films.